

# Master Thesis

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Theme:  
Evaluation and Design of a Single  
microcontrolled POCSAG Decoder

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To my parents

# Preamble

This Master Thesis is the final part of a development obtaining a complete POCSAG receiver containing RF stage, signal processing module and microcontroller unit.

Special featured by an outright assembler programming to ensure small memory usage and accurate comprehensible interface timing.

As a result of a previously available project study the RF receiver is part of this report.

Again the development work was done inside the author's company.

For advising and discussing I want to express my gratitude to Prof. Dr. Otto Parzhuber and Assistant Prof. Dr. Robert Bösnecker.

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Thomas Miehling

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## Chapter 8

### Subsumption

This project was able to show the capabilities of a cheap and powerful PIC microcontroller doing the whole POCSAG decoding, relay steering and data output. More feasibilities to integrate is highly impossible into the used chip within this project. For programme memory as well as port pins we have to chose the next greater type.

But nevertheless the stationary receiver is built up flexibly so that the microcontroller print can be changed very easily for future needs.

A reliable replacement for the Phillips chipset is now available and software can easily be adapted to users' needs. Compared to the original chipset's price the naked microcontroller hardware costs only a trickle. The discrete built receiver has even a higher sensitivity compared with Phillips' chipset. We have shown this in [7].

The next enhancement will be the implementation of IDEA decryption to be also in the position to serve all encrypted POCSAG nets. Interesting especially because of the patent expiration at last in may 2011. From this time on IDEA is not sourced any more with any kind of license fees.

# Bibliography

- [1] *Error Detection and Correction of MPT1327 Formatted Messages*. Consumer Microcircuits. Ltd., 1994.
- [2] *PIC16F627A/628A/648A Data Sheet FLASH-Based 8-bit CMOS Microcontrollers*. Microchip Technology Inc., 2002.
- [3] *Technische Richtlinie der Behörden und Organisation mit Sicherheitsaufgaben (BOS) - Geräte für die digitale Funkalarmierung*. Ausschuss für Informations- und Kommunikationswesen und Zentralprüfstelle für drahtlose Fernmeldegeräte bei der Landesfeuerwehrschule Baden-Württemberg. Unterausschuss Information und Kommunikation (UA IuK) des Arbeitskreises II "Innere Sicherheit" der Arbeitsgemeinschaft der Innenministerien der Länder, 2005.
- [4] Stan D'Souza. *AN556 - Implementing a Table Read*. Microchip Technology Inc., 2002.
- [5] N.J.A. Sloane F.J. MacWilliams. *The Theory of Error-Correcting Codes*. North-Holland.
- [6] Gavin J. Hurlbut. *Design and Implementation of a Bit Error Rate Tester*. University of Waterloo, 2002.
- [7] Thomas Miebling. *Entwurf, Design und Realisierung eines HF-Überlagerungsempfängers*. University of Applied Sciences Munich, 2008.
- [8] Joy A. Thomas Thomas M. Cover. *Elements of Information Theory*. John Wiley & Sons, 1991.
- [9] E. J. Weldon W. W. Peterson. *Error-Correcting-Codes*. MIT press, 1972.